AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. – 18. (Canceled).

19. (Currently amended) A random access memory (RAM) capacitor in a shallow trench isolation comprising ~~comprised of~~:

a substrate having said shallow trench isolation surrounding active device areas;

a pad oxide layer on said substrate;

a first hard-mask layer on said pad oxide layer;

recesses in said first hard-mask layer, said pad oxide layer, and partially within said shallow trench isolation and said recesses extending under said first hard-mask layer to said substrate and said recesses having ~~a bottle-shape~~ lower portions and upper portions, said upper portions being narrower than said lower portions;

a conformal first conducting layer in said recesses for capacitor bottom electrodes;

an interelectrode dielectric layer over said bottom electrodes; and

a conformal second conducting layer that fills said recesses sufficiently thick to form a planar surface over said recesses.

20. (Currently amended) The structure of claim 19, further comprising:

a ~~planar~~ second hard-mask layer over said second conducting layer; ~~and said second hard-mask layer and~~

~~said second conducting layer having a pattern to form capacitor top electrodes having sidewall spacers;~~

a gate oxide on said substrate; and

~~a third conducting layer patterned for~~ gate electrodes ~~on~~ over said substrate ~~and over said RAM capacitors~~;

said second conducting layer having a pattern to form capacitor top electrodes having sidewall spacers.

21. (Original) The structure of claim 19, wherein said substrate is a silicon substrate.

22. (Original) The structure of claim 19, wherein said pad oxide is silicon oxide and has a thickness of between about 50 and 300 Angstroms.

23. (Original) The structure of claim 19, wherein said first hard-mask layer is silicon nitride and has a thickness of between about 100 and 500 Angstroms.

24. (Original) The structure of claim 19, wherein said first conducting layer is a material selected from the group that includes polysilicon, TiN, WN, MoN, WSiN, TiW, TaM, and Ta.

25. (Original) The structure of claim 19, wherein said first conducting layer has a thickness of between about 100 and 500 Angstroms.

26. (Original) The structure of claim 19, wherein said inter-electrode dielectric layer is silicon oxide/silicon nitride/silicon oxide and has a thickness of between about 30 and 100 Angstroms.

27. (Original) The structure of claim 19, wherein said second conducting layer is a material selected from the group that includes polysilicon, TIN, WN, MoN, WSiN, TiW, TaM, and Ta.

28. (Currently amended) The structure of claim [[20]] 29, wherein said second hard-mask layer is silicon oxynitride and has a thickness of between about 100 and 800 Angstroms.

29. (Currently amended) A random access memory (RAM) capacitor in a shallow trench isolation comprising:

a substrate having said shallow trench isolation surrounding active device areas;

a pad oxide layer on said substrate;

a first hard-mask layer on said pad oxide layer;

recesses in said first hard-mask layer, said pad oxide layer and partially within said shallow trench isolation, said recesses extending under said first hard-mask layer to said substrate, said recesses having a bottle-shape;

a conformal first conducting layer in said recesses for capacitor bottom electrodes;

an inter-electrode dielectric layer over said bottom electrodes; and

a conformal second conducting layer that fills said recesses sufficiently thick to form a planar surface over said recesses ~~The structure of claim 20~~,

wherein said sidewall spacers are an insulating material.

30. (Currently amended) The structure of claim [[20]] 29, wherein said gate oxide is a thermal oxide and has a thickness of between about 10 and 150 Angstroms.

31. (Currently amended) The structure of claim [[20]] 29, wherein said third conducting layer is a material selected from the group that includes polysilxcon, TiN, WN, MoN, WSiN, TiW, TaN, and Ta.

32. (Currently amended) The structure of claim [[20]] 29, wherein said third conducting layer has a thickness of between about 500 and 3000 Angstroms.

33. (New) The structure of claim 29, wherein said pad oxide is silicon oxide and has a thickness of between about 50 and 300 Angstroms.

34. (New) The structure of claim 29, wherein said first hard-mask layer is silicon nitride and has a thickness of between about 100 and 500 Angstroms.

35. (New) The structure of claim 29, wherein said first conducting layer is a material selected from the group that includes polysilicon, TiN, WN, MoN, WSiN, TiW, TaM, and Ta.

36. (New) The structure of claim 29, wherein said first conducting layer has a thickness of between about 100 and 500 Angstroms.

37. (New) The structure of claim 29, wherein said inter-electrode dielectric layer is silicon oxide/silicon nitride/silicon oxide and has a thickness of between about 30 and 100 Angstroms.

38. (New) The structure of claim 29, wherein said second conducting layer is a material selected from the group that includes polysilicon, TIN, WN, MoN, WSiN, TiW, TaM, and Ta.